What is claimed is:

1. An on-chip testing apparatus comprising:

a test pattern generator to generate test data for a plurality of testing channels; and

a weight selector coupled to said test pattern generator, said weight selector to store weighting values to bias data for at least one of said testing channels.

2. The apparatus of claim 1 wherein said weight selector includes a weight storage register to store said weighting values and said weight selector is to selectively bias individual bits of said test data.

3. The apparatus of claim 2 wherein said weight selector causes a reduction in power usage when said weight storage registers store weighting values to bias data for at least one testing channels to one of all 0 values and all 1 values.

4. An on-chip testing apparatus comprising:

a test pattern generator to generate test data for a plurality of testing channels;

clock control logic to selectively supply scan clocking signals to said testing channels, such that said scan clocking signals scan said test data into said testing channels.

5. The apparatus of claim 4 further comprising:

a signature register coupled to said testing channels to receive data from said testing channels when said scan clocking signals are supplied to said testing channels.

6. An on-chip testing apparatus comprising:

clock control logic to selectively supply functional clocking signals to a plurality of testing channels, such that said functional clocking signals operate logic in said testing channels.

7. The apparatus of claim 6 wherein said clock control logic further includes clock control logic to generate stop clock signals to said testing channels.

8. The apparatus of claim 7 wherein said clock control logic further includes a scan counter counting said functional clocking signals and a breakpoint stop register to store a value such that at least one of said stop clock signals is generated when a count in said scan counter matches a value in said breakpoint stop register.

9. An on-chip testing apparatus comprising:

channel filtering logic to receive data from a plurality of testing channels, said channel filtering logic to mask output data from a selected testing channel.

10. The apparatus of claim 9 further comprising:

a signature register coupled to said channel filtering logic to receive said data.

11. A method of performing on-chip testing comprising:

generating test data in a test pattern generator for a plurality of testing channels; and

biasing said test data for at least one of the testing channels with weighting values stored in a weight selector coupled to said test pattern generator.

12. The method of claim 11 wherein in biasing said test data, said biasing is performed selectively on individual bits of said test data.

13. The method of claim 12 wherein in biasing said test data all of said test data is biased to one of all 0 values and all 1 values.

14. A method of performing on-chip testing comprising:

generating test data in a test pattern generator for a plurality of testing channels; and

selectively supplying scan clocking signals to said testing channels to scan said test data into said testing channels.

15. The method of claim 14 further comprising:

supplying said data received from said testing channels to a signature register coupled to said testing channels.

16. A method of performing on-chip testing comprising:

selectively supplying functional clocking signals to a plurality of testing channels to operate logic in said testing channels.

17. The method of claim 16 further comprising:

selectively generating stop clock signals to said testing channels.

18. The method of claim 17 further comprising:

counting said functional clocking signals in a scan counter; such that at least one of said stop clock signals is generated when a count in said scan counter matches a value in a breakpoint stop register.

19. A method of performing on-chip testing comprising:

receiving data from a plurality of testing channels at channel filtering logic; and

masking output data from a selected testing channel.

20. The method of claim 19 further comprising:

supplying masked output data from said channel filtering logic to a signature register coupled to said channel filtering logic.